ABSTRACT

A memory chip (20) includes a main memory cell (27); a row-wise redundant memory cell (28) and a column-wise redundant memory cell (29) for redeeming a defect present in the main memory (27); an identification number designation terminal (26) for storing an identification number corresponding to the main memory cell (27); an address terminal (21) for receiving the identification number; and a redundant row selector circuit (30) and a redundant column selector circuit (31) for performing allocation so as to replace a defective memory space of the main memory cell (27) with a memory space of the redundant memory cells (27, 28). The redundant selector circuits (30, 31) allocate a memory space corresponding to the defect of the main memory cell (27) to the redundant memory cells (28, 29) when the identification number received from the address terminal (21) coincides with the identification number of the identification number specification terminal (26).